ANALOG DEVICES

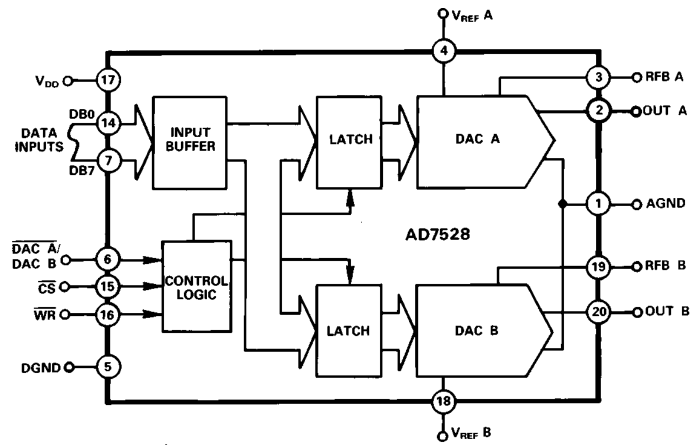
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7528

FEATURES
On-Chip Latches for Both DACs
+5 V to +15 V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch Free (Protection Schottkys not Required)

APPLICATIONS
Digital Control of:
- **Gain/Attenuation**
- **Filter Parameters**
- **Stereo Audio Circuits**
- **X-Y Graphics**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5 V to +15 V power supply, dissipating only 20 mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.

2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin DIP, SOIC, PLCC or LCCC.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7528JN	–40°C to +85°C	±1 LSB	±4 LSB	N-20
AD7528KN	–40°C to +85°C	±1/2 LSB	±2 LSB	N-20
AD7528LN	–40°C to +85°C	±1/2 LSB	±1 LSB	N-20
AD7528JP	–40°C to +85°C	±1 LSB	±4 LSB	P-20A
AD7528KP	–40°C to +85°C	±1/2 LSB	±2 LSB	P-20A
AD7528LP	–40°C to +85°C	±1/2 LSB	±1 LSB	P-20A
AD7528JR	–40°C to +85°C	±1 LSB	±4 LSB	R-20
AD7528KR	–40°C to +85°C	±1/2 LSB	±2 LSB	R-20
AD7528LR	–40°C to +85°C	±1/2 LSB	±1 LSB	R-20
AD7528AQ	–40°C to +85°C	±1 LSB	±4 LSB	Q-20
AD7528BQ	–40°C to +85°C	±1/2 LSB	±2 LSB	Q-20
AD7528CQ	–40°C to +85°C	±1/2 LSB	±1 LSB	Q-20
AD7528SQ	–55°C to +125°C	±1 LSB	±4 LSB	Q-20
AD7528TQ	–55°C to +125°C	±1/2 LSB	±2 LSB	Q-20
AD7528UQ	–55°C to +125°C	±1/2 LSB	±1 LSB	Q-20
AD7528SE	–55°C to +125°C	±1 LSB	±4 LSB	E-20A
AD7528TE	–55°C to +125°C	±1/2 LSB	±2 LSB	E-20A
AD7528UE	–55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship side-brazed ceramic in lieu of cerdip. Parts will be marked with cerdip designator "Q."
[2]Processing to MIL-STD-883C, Class B is available. To order, add suffix "/883B" to part number. For further information, see Analog Devices' 1990 Military Products Databook.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

REV. A

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AD7528–SPECIFICATIONS (V_{REF} A = V_{REF} B = +10 V; OUT A = OUT B = 0 V unless otherwise noted)

Parameter	Version[1]	V_{DD} = +5 V		V_{DD} = +15 V		Units	Test Conditions/Comments
		T_A = +25°C	T_{MIN}, T_{MAX}	T_A = +25°C	T_{MIN}, T_{MAX}		
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±1/2	±1/2	±1/2	±1/2	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5
Gain Temperature Coefficient[4]							
ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF}A, V_{REF}B)	All	8	8	8	8	kΩ min	Input Resistance TC = –300 ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11 kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage							
V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage							
V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current							
I_{IN}	All	±1	±10	±1	±10	µA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, $\overline{DAC\ A}$/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time							
t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time							
t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time							
t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time							
t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time							
t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time							
t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	µA max	All Digital Inputs 0 V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5 V		V_{DD} = +15 V		Units	Test Conditions/Comments
		T_A = +25°C	T_{MIN}, T_{MAX}	T_A = +25°C	T_{MIN}, T_{MAX}		
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2 LSB. Out A/Out B load = 100 Ω. $\overline{WR}$ = $\overline{CS}$ = 0 V. DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10 V OUT A, OUT B Load = 100 Ω C_{EXT} = 13 pF $\overline{WR}$ = $\overline{CS}$ = 0 V DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	160		440		nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT}A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT}B		50	50	50	50	pF max	
C_{OUT}A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT}B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	–70	–65	–70	–65	dB max	V_{REF} A, V_{REF} B = 20 V p-p Sine Wave
V_{REF} B to OUT B		–70	–65	–70	–65	dB max	@ 100 kHz

Parameter	Version[1]	V_{DD} = +5 V T_A = +25°C	V_{DD} = +5 V T_{MIN}, T_{MAX}	V_{DD} = +15 V T_A = +25°C	V_{DD} = +15 V T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
CHANNEL-TO-CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	–77		–77		dB typ	V_{REF} A = 20 V p-p Sine Wave @ 100 kHz V_{REF} B = 0 V see Figure 6.
V_{REF}B to OUT A		–77		–77		dB typ	V_{REF} A = 20 V p-p Sine Wave @ 100 kHz V_{REF} A = 0 V see Figure 6.
DIGITAL CROSSTALK	All	30		60		nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	–85		–85		dB typ	V_{IN} = 6 V rms @ 1 kHz

NOTES
[1]Temperature Ranges are J, K, L Versions: –40°C to +85°C
A, B, C Versions: –40°C to +85°C
S, T, U Versions: –55°C to +125°C
[2]Specifications applies to both DACs in AD7528.
[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1 nA.
[4]Guaranteed by design but not production tested.
[5]These characteristics are for design guidance only and are not subject to test.
[6]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . 0 V, +17 V
V_{DD} to DGND . . . . 0 V, +17 V
AGND to DGND . . . . V_{DD} + 0.3 V
DGND to AGND . . . . V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . –0.3 V, V_{DD} + 0.3 V
V_{PIN2}, V_{PIN20} to AGND . . . . –0.3 V, V_{DD} + 0.3 V
V_{REF} A, V_{REF} B to AGND . . . . ±25 V
V_{RFB} A, V_{RFB} B to AGND . . . . ±25 V
Power Dissipation (Any Package) to +75°C . . . . 450 mW
Derates above +75°C by . . . . 6 mW/°C
Operating Temperature Range
Commercial (J, K, L) Grades . . . . –40°C to +85°C
Industrial (A, B, C) Grades . . . . –40°C to +85°C
Extended (S, T, U) Grades . . . . –55°C to +125°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7528, ideal maximum output is V_{REF} – 1 LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

Digital to Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

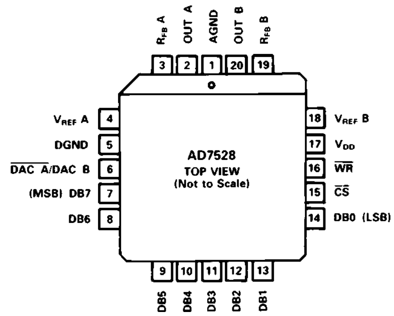
Propagation Delay:
This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

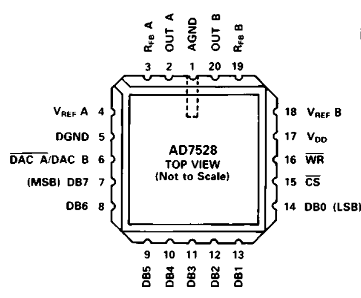
Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

PIN CONFIGURATIONS

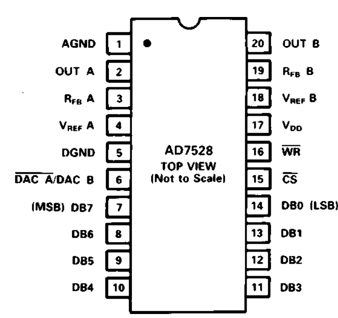
PLCC



LCCC



DIP, SOIC



INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

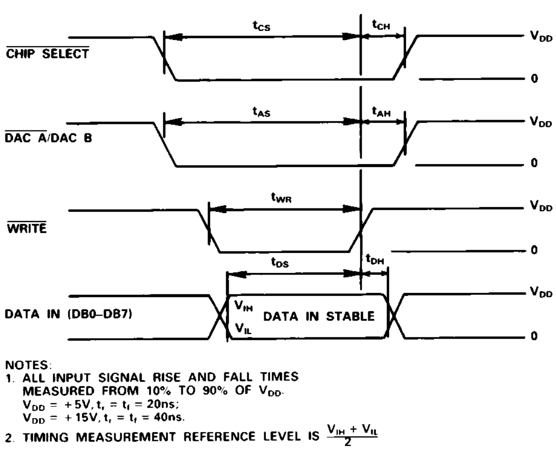
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Mode Selection Table

$\overline{\text{DAC A}}$/DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State; H = High State; X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



CIRCUIT INFORMATION—D/A SECTION

The AD7528 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

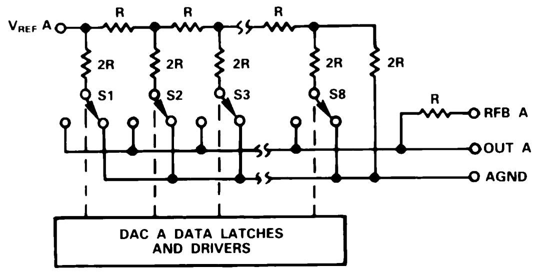


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0s code) from 0.8 R to 2 R. R is typically 11 kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50 pF to 120 pF depending upon the digital input. g(V_{REF} A, N) is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

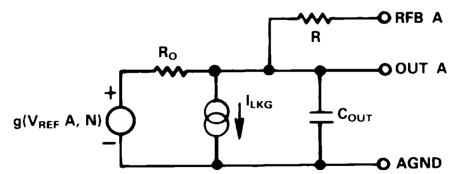


Figure 2. Equivalent Analog Output Circuit of DAC A

CIRCUIT INFORMATION–DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the AD7528 is operated with V_{DD} = 5 V, the buffer converts TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7528 may be operated with any supply voltage in the range 5 ≤ V_{DD} ≤ 15 volts. With V_{DD} = +15 V the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V.

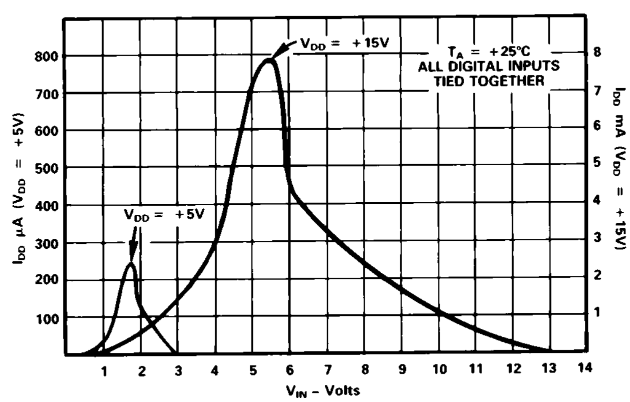
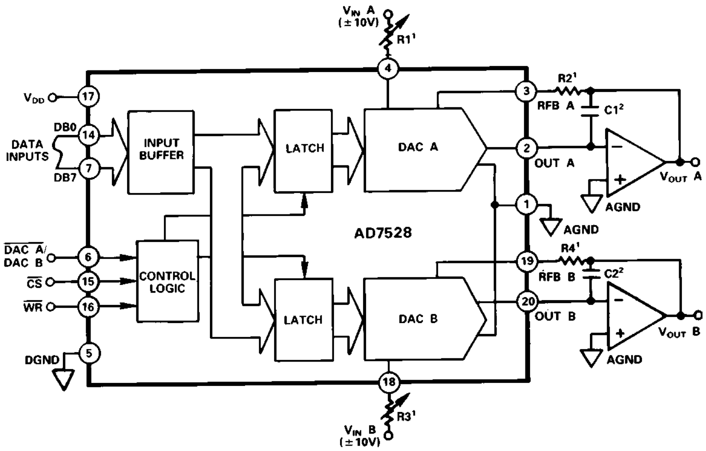
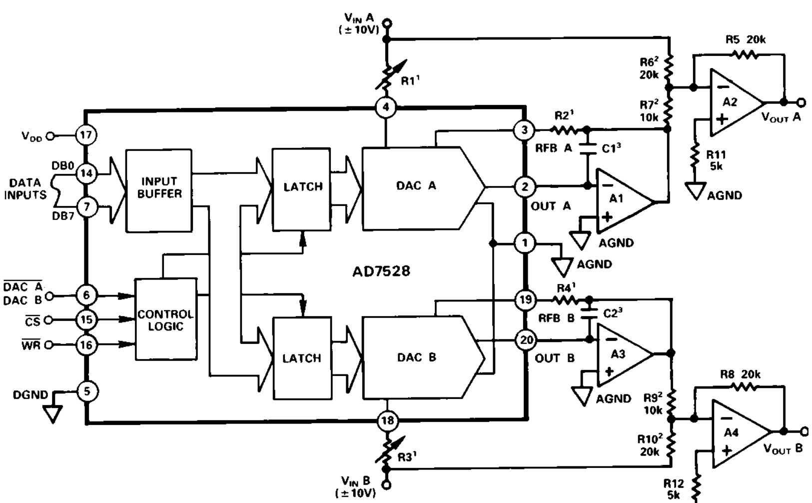


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5 V and +15 V



NOTES:
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
[2]C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication); See Table I



NOTES:
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES. ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH. ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
[2]MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
[3]C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication); See Table II

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note: 1 LSB = $\left(2^{-8}\right)\left(V_{IN}\right) = \frac{1}{256}\left(V_{IN}\right)$

Table II. Bipolar (Offset Binary) Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{128}{128}\right)$

Note: 1 LSB = $\left(2^{-7}\right)\left(V_{IN}\right) = \frac{1}{128}\left(V_{IN}\right)$

Table III. Recommended Trim Resistor Values vs. Grade

Trim Resistor	J/A/S	K/B/T	L/C/U
R1; R3	1 k	500	200
R2; R4	330	150	82

APPLICATIONS INFORMATION

Application Hints

To ensure system performance consistent with AD7528 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the AD7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7528. In more complex systems where the AGND–DGND intertie is on the backplane, it is recommended that diodes be connected in inverse parallel between the AD7528 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
3. HIGH FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

DYNAMIC PERFORMANCE

The dynamic performance of the two DACs in the AD7528 will depend upon the gain and phase characteristics of the output amplifiers together with the optimum choice of the PC board layout and decoupling components. Figure 6 shows the relationship between input frequency and channel to channel isolation. Figure 7 shows a printed circuit layout for the AD7528 and the AD644 dual op-amp which minimizes feedthrough and crosstalk.

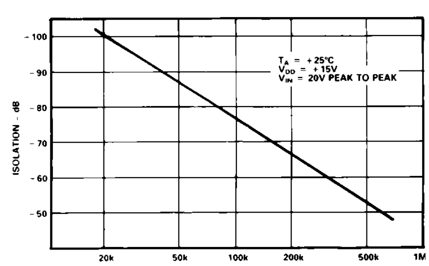


Figure 6. Channel to Channel Isolation

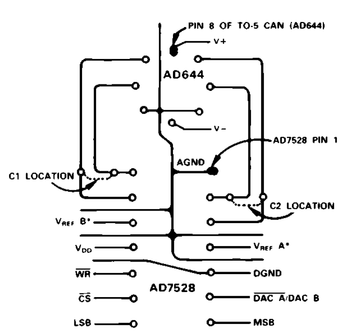


Figure 7. Suggested PC Board Layout for AD7528 with AD644 Dual Op Amp

SINGLE SUPPLY APPLICATIONS

The AD7528 DAC R-2R ladder termination resistors are connected to AGND within the device. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 8 shows a circuit which provides two +5 V to +8 V analog outputs by biasing AGND +5 V up from DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1 and R1 is adjusted until the V_{REF} A and V_{REF} B inputs are at +2 V. The two analog output voltages range from +5 V to +8 V for DAC codes 00000000 to 11111111.

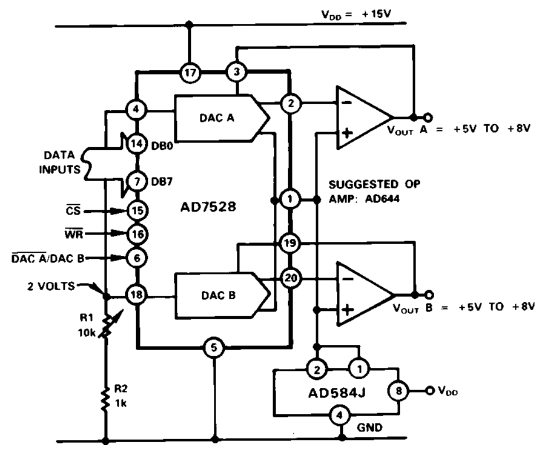


Figure 8. AD7528 Single Supply Operation

Figure 9 shows DAC A of the AD7528 connected in a positive reference, voltage switching mode. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to retain specified linearity, V_{IN} must be in the range 0 to +2.5 V and the output buffered or loaded with a high impedance, see Figure 10. Note that the input voltage is connected to the DAC OUT A and the output voltage is taken from the DAC V_{REF} A pin.

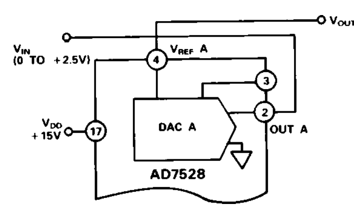


Figure 9. AD7528 in Single Supply, Voltage Switching Mode

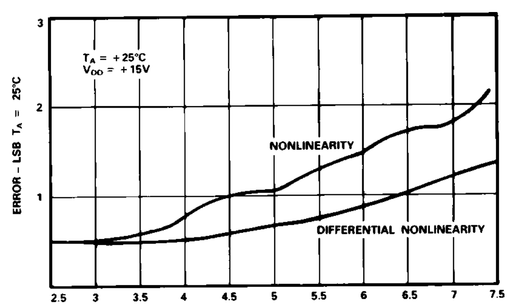


Figure 10. Typical AD7528 Performance in Single Supply Voltage Switching Mode (K/B/T, L/C/U Grades)

MICROPROCESSOR INTERFACE

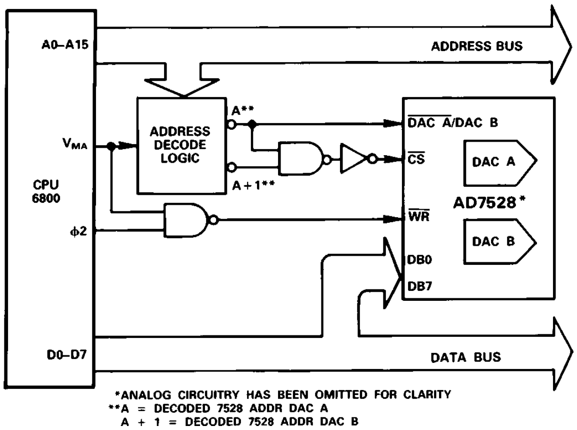


Figure 11. AD7528 Dual DAC to 6800 CPU Interface

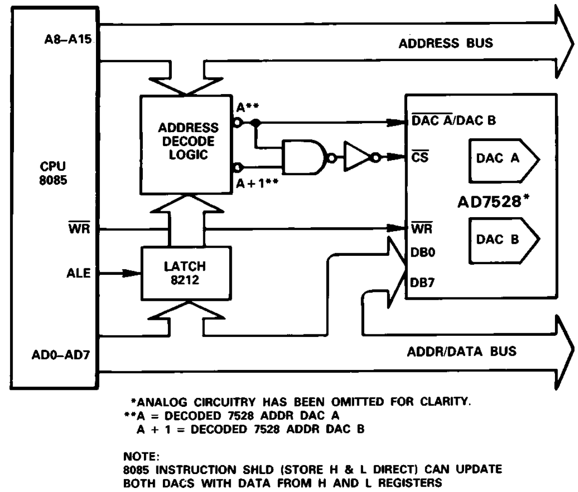


Figure 12. AD7528 Dual DAC to 8085 CPU Interface

PROGRAMMABLE WINDOW COMPARATOR

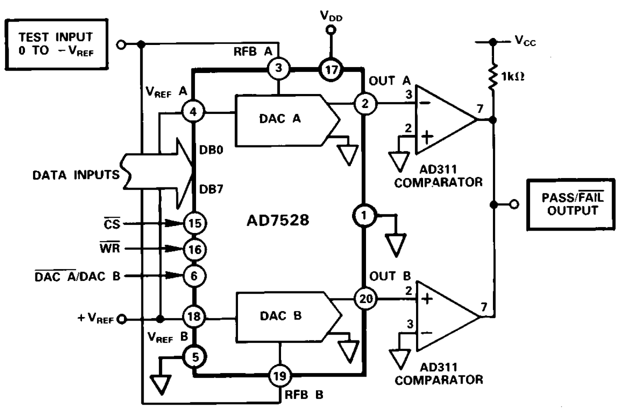


Figure 13. Digitally Programmable Window Comparator (Upper and Lower Limit Detector)

In the circuit of Figure 13 the AD7528 is used to implement a programmable window comparator. DACs A and B are loaded with the required upper and lower voltage limits for the test, respectively. If the test input is not within the programmed limits, the pass/fail output will indicate a fail (logic zero).

PROGRAMMABLE STATE VARIABLE FILTER

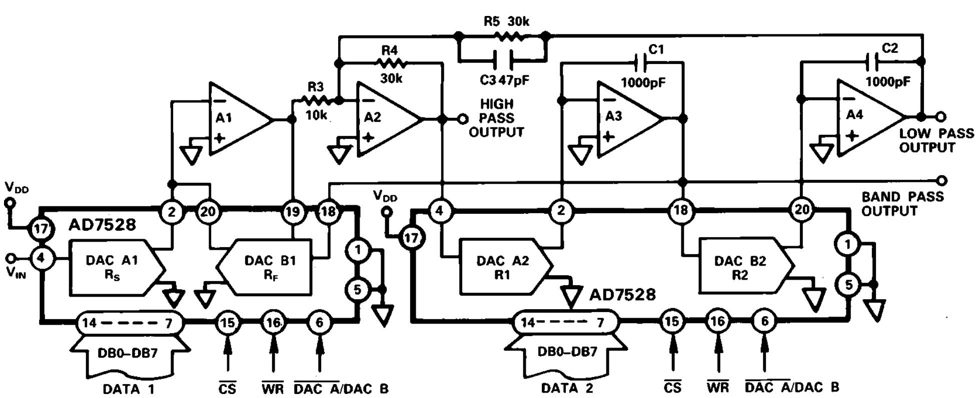


Figure 14. Digitally Controlled State Variable Filter

CIRCUIT EQUATIONS

$$C_1 = C_2, R_1 = R_2, R_4 = R_5$$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \times \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals

$$\frac{256 \times (DAC\ Ladder\ resistance)}{DAC\ Digital\ Code}$$

In this state variable or universal filter configuration (Figure 14) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cutoff frequency, fc. DACs A2 and B2 must track accurately for the simple expression for fc to hold. This is readily accomplished by the AD7528. Op amps are 2 × AD644. C3 compensates for the effects of op amp gain bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is fc = 0 to 15 kHz and Q = 0.3 to 4.5.

DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

In this configuration the AD7528 functions as a 2-channel digitally controlled attenuator. Ideal for stereo audio and telephone signal level control applications. Table IV gives input codes vs. attenuation for a 0 to 15.5 dB range.

$$\text{Input Code} = 256 \times 10 \exp\left(-\frac{\text{Attenuation, dB}}{20}\right)$$

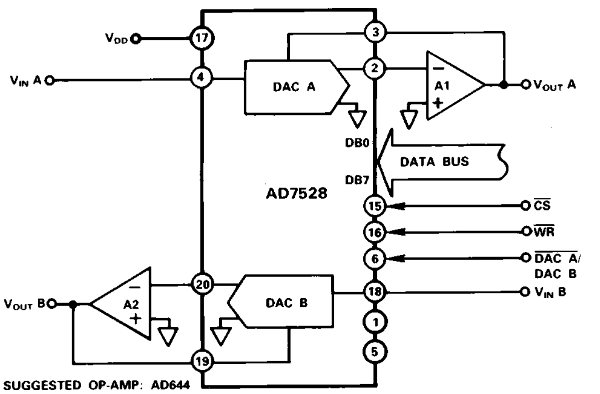


Figure 15. Digitally Controlled Dual Telephone Attenuator

Table IV. Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 15

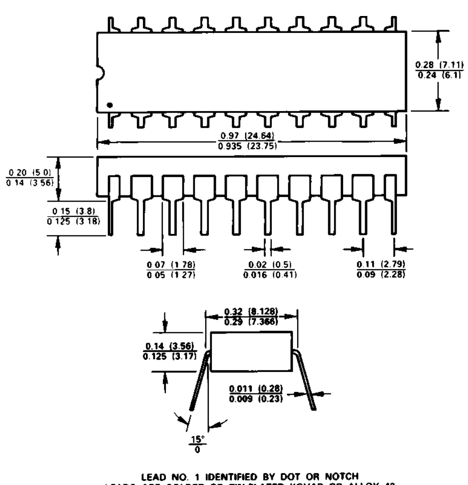
Attn. dB	DAC Input Code	Code In Decimal	Attn. dB	DAC Input Code	Code In Decimal
0.0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

For further applications information the reader is referred to Analog Devices Application Note on the AD7528.

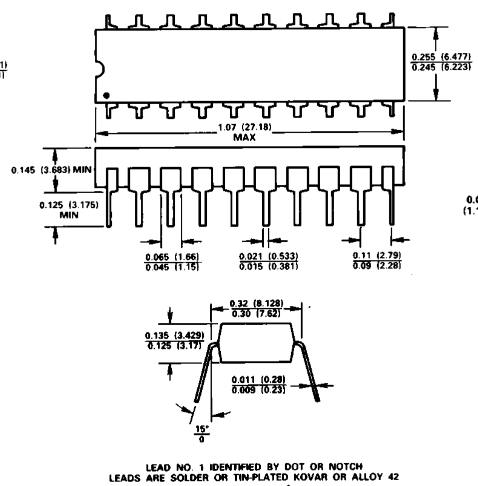
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

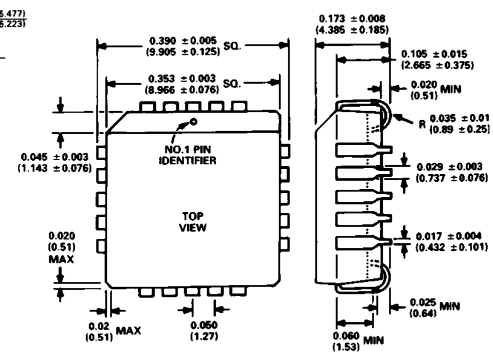
20-Pin Cerdip (Q-20)



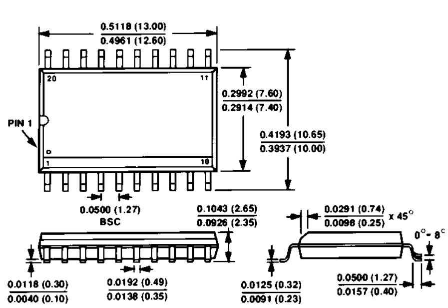
20-Pin Plastic DIP (N-20)



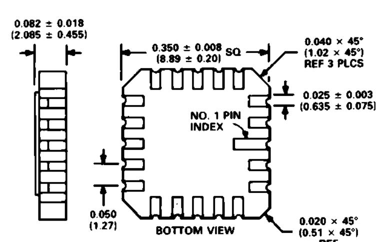
20-Terminal Plastic Leaded Chip Carrier (P-20A)



20-Pin SOIC (R-20)



20-Terminal Leadless Ceramic Chip Carrier (E-20A)



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